CLAIMS

1. A display device comprising an array of current-addressed display pixels (1) and driver circuitry for providing pixel drive currents to the pixels of the array, wherein the driver circuitry comprises a plurality of current drive circuits, each having an output transistor arrangement, wherein the output transistor arrangement comprises a plurality of output transistors (70,72,74) in parallel, and wherein within each current drive circuit, one or more of the output transistors (70,72,74) can be selected in order to provide desired output characteristics.

2. A device as claimed in claim 1, wherein the current drive circuits are at least partially integrated onto the substrate of the array of display pixels..

3. A device as claimed in claim 2, wherein the display pixels comprise active matrix display pixels, each comprising a pixel circuit having at least one thin film transistor (22).

4. A device as claimed in claim 3, wherein the thin film transistor (22) comprises a polysilicon TFT, and wherein the output transistors comprise polysilicon TFTs on the same substrate as the display pixels.

5. A device as claimed in claim 4, wherein the thin film transistor (22) and the output transistors (70,72,74) comprise low temperature polysilicon TFTs.

6 A device as claimed where the output transistors of the current drive circuits are made in the same process as the array of current-addressed display pixels but on a different substrate.

7. A device as claimed in any preceding claim, wherein one or more of the output transistors are selected by breaking a fusible link (78) thereby to disconnect the non-selected output transistors.

8. A device as claimed in any one of claims 1 to 6, wherein one or more of the output transistors (70,72,74) are selected by electrically connecting them in parallel.

9. A device as claimed in claim 8, wherein one or more of the output transistors are selected by further switches (80,84) which either connect their gate to a common gate control line (82) for the current drive circuit or to a deselect line.

10. A device as claimed in claim 7, 8 or 9, wherein one of the output transistors (70) is a main output transistor and the others (72,74) are fine tuning transistors having smaller channel widths than the main output transistor.

11. A device as claimed in claim 10, wherein the channel width/length ratio of each fine tuning transistor (72,74) is less than 1/25 of the width/length ratio of the main output transistor (70).

12. A device as claimed in claim 7, 8 or 9, wherein only one of the output transistors (70,72,74) is selected, and the channel width/length ratios of all of the output transistors vary by less than 10%.

13. A device as claimed in any preceding claim, wherein the current-addressed display pixels comprise electroluminescent display pixels.

14. A device as claimed in claim 13, wherein the current-addressed display pixels each comprise an organic LED.

15. A method of tuning driver circuitry for providing pixel drive currents to the pixels of a display device having an array of current-addressed display

pixels, the driver circuitry comprising a plurality of current drive circuits, the method comprising:

providing each current drive circuit with an output transistor arrangement comprising a plurality of output transistors (70,72,74) in parallel;

selecting one or more of the output transistors (70,72,74) to provide desired output characteristics for the current drive circuit.

16. A method as claimed in claim 15, wherein the selection is performed based on an analysis of the output characteristics of the display device for a given default selection of the output transistors (70,72,74).

17. A method as claimed in claim 16, wherein the analysis of the output characteristics is performed by monitoring the light output of the display using an image sensor and analysing the sensed image.

18. A method as claimed in claim 16 or 17, wherein the selection comprises breaking a fusible link (78) thereby to disconnect the non-selected output transistors.

19. A method as claimed in claim 18, wherein one of the output transistors (70) is a main output transistor and the others are fine tuning transistors (72,74) having smaller channel width/length ratios than the main output transistor, and the method comprises selecting the main output transistor (70) and 0, 1 or more of the fine tuning transistors (72,74).

20. A method as claimed in claim 18, wherein the channel width/length ratios of all of the output transistors vary by less than 10%, and the method comprises selecting only one of the output transistors (70,72,74).

21. A method as claimed in claim 16 or 17, wherein the selection comprises electrically connecting the selected transistors in parallel.